07/17/98 JC600 U.S. PTO

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Please type a plus sign (+) inside this box → [+]

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	MI22-587	Total Pages	
First Named Inventor or Application Identifier	J. Dennis Keller et al.		
Express Mail Label No.	EL054830156		

U.S. PTO 09/118359 07/17/98

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification *(preferred arrangement set forth below)* [Total Pages 23]
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [Total Sheets 4]
4. Oath or Declaration [Total Pages 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [X] Other: Check for $1,378.00

17. If a **CONTINUING APPLICATION,** *check appropriate box and supply the requisite information:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: ______

18. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* 021567 *(Insert Customer No. or Attach bar code label here)* or [X] *Correspondence address below*

NAME	Lance R. Sadler 7/17/98				
ADDRESS	Wells, St. John, Roberts, Gregory & Matkin, P.S. 601 West First Ave., Suite 1300				
CITY	Spokane	STATE	WA	ZIP CODE	99201-3828
COUNTRY	U.S.A.	TELEPHONE	(509) 624-4276	FAX	(509) 838-3424

EL054830156

PTO/SB/17 (12-97)
Approved use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL

Note. Effective October 1, 1997.
Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 1,378.00

Complete if Known	
Application Number	Unknown
Filing Date	Filed Herewith
First Named Inventor	J. Dennis Keller et al.
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	MI22-587

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 23-0925

Deposit Account Name: Wells, St. John et al.

[X] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

[ ] Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2. [X] Payment Enclosed:
[X] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
~~101~~	~~790~~	201	395	Utility filing fee	790
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 790

2. CLAIMS

			Extra		Fee from below		Fee Paid
Total Claims	40	-20 =	20	X	22	=	440
Independent Claims	7	- 3 =	4	X	82	=	328
Multiple Dependent Claims			0	X		=	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim
109	82	209	41	Reissue independent claims over original patent
110	22	210	11	Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 768

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	0
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	0
139	130	139	130	Non-English specification	0
147	2,520	147	2,520	For filing a request for reexamination	0
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	0
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	0
115	110	215	55	Extension for reply within first month	0
116	400	216	200	Extension for reply within second month	0
117	950	217	475	Extension for reply within third month	0
118	1,510	218	755	Extension for reply within fourth month	0
128	2,060	228	1,030	Extension for reply within fifth month	0
119	310	219	155	Notice of Appeal	0
120	310	220	155	Filing a brief in support of an appeal	0
121	270	221	135	Request for oral hearing	0
138	1,510	138	1,510	Petition to institute a public use proceeding	0
140	110	240	55	Petition to revive - unavoidable	0
141	1,320	241	660	Petition to revive - unintentional	0
142	1,320	242	660	Utility issue fee (or reissue)	0
143	450	243	225	Design issue fee	0
144	670	244	335	Plant issue fee	0
122	130	122	130	Petitions to the Commissioner	0
123	50	123	50	Petitions related to provisional applications	0
126	240	126	240	Submission of Information Disclosure Stmt	0
581	40	581	40	Recording each patent assignment per property (times number of properties)	40
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	0
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	0
Other fee (specify) ________					0
Other fee (specify) ________					0

* Reduced by Basic Filing Fee Paid

SUBTOTAL(3) ($) 40

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	Lance R. Sadler			Reg. Number	38,605
Signature	[signature]	Date	7/1/98	Deposit Account User ID	

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

EL054830156

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Methods Of Enhancing Data Retention Of A Floating Gate Transistor, Methods Of Forming Floating Gate Transistors, And Floating Gate Transistors

* * * * *

INVENTORS

J. Dennis Keller
Roger R. Lee

ATTORNEY'S DOCKET NO. MI22-587

EL054830156

TECHNICAL FIELD

This invention relates to floating gate transistors and methods of forming the same. This invention also relates to methods of enhancing data retention of floating gate transistors.

BACKGROUND OF THE INVENTION

Floating gate transistors are utilized in some semiconductor memory cells. One type of memory cell that uses a floating gate transistor is a flash erasable and programmable read only memory (EPROM). A floating gate transistor typically includes a tunnel dielectric layer, a floating gate, an interlayer dielectric and a control gate or word line. Source/drain regions are formed operatively adjacent the floating gate and within semiconductive substrate material. A floating gate transistor can be placed in a programmed state by storing charge on the floating gate of the floating gate transistor. Typically, a large voltage, e.g. 25 volts, between the control gate and the substrate allow some electrons to cross the interlayer dielectric and charge the floating gate. The "data retention" of a floating gate transistor refers to the ability of the transistor to retain its charge over a period of time. Charge can be lost, undesirably, through electron migration from the floating gate through various adjacent materials. One problem which has confronted the industry is electron migration through the interlayer dielectric material immediately above the floating gate. The thickness of the interlayer dielectric material has an impact

on the ability of a floating gate to retain its charge. Thinner regions of the interlayer dielectric material provide undesired migration paths for electrons to leave the programmed floating gate relative to other thicker regions of the interlayer dielectric material. Hence, non-uniformity in the thickness of the interlayer dielectric material is undesirable.

A contributing factor to a non-uniformly thick interlayer dielectric material is the presence of a large number of grain boundaries at the interlayer dielectric/floating gate interface. Conductive doping of the floating gate, as is desirable, undesirably increases the number of interface grain boundaries, which in turn, increases the chances of having a non-uniformly thick interlayer dielectric.

This invention grew out of concerns associated with improving the data retention characteristics of floating gate transistors.

SUMMARY OF THE INVENTION

Floating gate transistors and methods of forming the same are described. In one implementation, a floating gate is formed over a substrate. The floating gate has an inner first portion and an outer second portion. Conductivity enhancing impurity is provided in the inner first portion to a greater concentration than conductivity enhancing impurity in the outer second portion. In another implementation, the floating gate is formed from a first layer of conductively doped semiconductive material and a second layer of substantially undoped semiconductive material. In another implementation, the floating gate

is formed from a first material having a first average grain size and a second material having a second average grain size which is larger than the first average grain size.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment at one processing step in accordance with the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 5.

Fig. 7 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 6.

Fig. 8 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a fragmentary portion of a semiconductor wafer is shown generally at 10 and comprises a semiconductive substrate 12. As used in this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Referring to Fig. 2, a layer 14 is formed over substrate 12 and constitutes a tunnel oxide layer.

Referring to Fig 3, a layer 16 is formed over substrate 12. In a preferred implementation, layer 16 constitutes a polysilicon layer which is formed to a first thickness t_1. Preferably, the polysilicon of layer 16 is undoped as formed and is subsequently doped, as through ion implantation, with conductivity enhancing impurity to a desired degree. According to one aspect, layer 16 is doped with a suitable impurity which is sufficient to define a sheet resistance of between 300 ohm/sq. and 400 ohm/sq. According to another aspect, first layer 16 is doped

with an impurity concentration which is greater than or equal to about 1 x $10^{18}cm^{-3}$. An exemplary concentration is between about 1 x $10^{18}cm^{-3}$ and 1 x $10^{20}cm^{-3}$, or greater. A suitable and preferred dopant or impurity is phosphorous. When phosphorous is utilized, the preferred sheet resistance is between about 600 ohm/sq. and 700 ohm/sq.

Alternately considered, layer 16 constitutes a first material or silicon-containing volume which is formed over the substrate and doped with a suitable impurity concentration to define a first average grain size. Accordingly, such silicon-containing volume has a first average grain boundary area per unit volume. An exemplary grain size is between about 50-100 nm, or about 10-25 grain boundaries in an erase area of 0.2 μm^2 to 0.4 μm^2.

Referring to Fig. 4, a second layer 18 is formed over the substrate 12 and first layer 16. Preferably, layer 18 is formed directly atop layer 16 and to a second thickness t_2. Preferably, second layer 18 constitutes a material such as polysilicon or amorphous silicon which is substantially undoped relative to first layer 16. The term "substantially undoped" as used within this document will be understood to mean having an impurity concentration which is less than 1 x $10^{18}cm^{-3}$. In accordance with one aspect of the invention, second layer 18 constitutes a second material which is formed over material of layer 16 to have a second average grain size which is larger than the first average grain size of layer 16. Accordingly, second layer 18 constitutes a second

silicon-containing volume having a second grain boundary area per unit volume which is less than the first grain boundary area per unit volume. An exemplary grain size is between about 100-200 nm, or greater than about 25 grain boundaries in an erase area of 0.2 μm^2 to 0.4 μm^2.

In a preferred implementation, the material of layers 16, 18, taken together, constitute material from which a floating gate of a floating gate transistor will be formed. Layers 16, 18 define an aggregate or combined thickness ($t_1 + t_2$). Accordingly to one aspect, the combined thickness of layers 16, 18 is less than or equal to about 1000 Angstroms. Such combined thickness can, however, range upward to around 1500 Angstroms or greater. The combined thickness can range downward as well. This is especially true as advances in scalability result in smaller floating gate dimensions. In one implementation, the first and second thicknesses are substantially the same. Accordingly, when the aggregate or combined thickness is around 1000 Angstroms, individual thicknesses t_1 and t_2 would be around 500 Angstroms. In another implementation, first and second thicknesses t_1 and t_2 can be different from one another. Accordingly, first thickness t_1 can constitute less than or equal to about 75% of the aggregate thickness. In another implementation, first thickness t_1 can constitute at least 25% of the aggregate or combined thickness of the floating gate. In yet another implementation, layer 16 can comprise between about 25-75% of the floating gate thickness. Where the aggregate thickness is

about 1000 Angstroms, the first thickness would be between 250-750 Angstroms. First thickness t_1 can be less than 550 Angstroms, or between 450 Angstroms and 550 Angstroms. In another implementation, the combined or aggregate thickness (t_1 + t_2) can equal around about 500 Angstroms, with thickness t_1 being equal to around 25-50 Angstroms. Other relative thickness relationships are of course possible.

Referring still to Fig. 4, layers 16 and 18 are subjected to suitable floating gate definition steps. In a first step, floating gate material 16, 18 is etched into and out of the plane of the page upon which Fig. 4 appears. Such effectively defines so-called floating gate wings which overlie field oxide which is not specifically shown in the Fig. 4 construction. The first etch partially forms a plurality of floating gates having respective inner first portions (layer 16) disposed proximate the substrate, and respective outer second portions (layer 18) disposed over the first portions.

Referring to Fig. 5, substrate 12 is subjected to suitable oxidizing conditions which are effective to form a first oxide layer 20 over second layer 18. Layer 20 constitutes a bottom oxide layer which is formed to a thickness of between about 50 Angstroms to 100 Angstroms.

Referring to Fig. 6, a layer 22 is formed over substrate 12 and preferably constitutes a nitride layer which is formed over first oxide layer 20. Substrate 12 is subsequently subjected to oxidizing conditions which are sufficient to form a second oxide layer 24 over nitride layer 22. Taken together, layers 20, 22, and 24 constitute an ONO

dielectric layer which constitutes a third layer 26 of dielectric material which is formed over the second silicon-containing volume or second layer 18. Other dielectric layers are possible.

Referring to Fig. 7, a fourth layer 28 is formed over third layer 26 and comprises a conductive material. In a preferred implementation, layer 28 constitutes a third layer of polysilicon which is formed over second oxide layer 24 and will constitute a conductive line for the floating gate transistor to be formed.

Referring to Fig. 8, the various layers of Fig. 7 are etched to provide a plurality of floating gate transistors 30, 32, 34, and 36. Such defines the remaining opposing edges of the floating gates of such transistors. The floating gate transistors are also provided with respective source/drain regions which are disposed laterally proximate the floating gates. In the illustrated example, individual source regions 38, 40 and a drain region 42 are shown. Additionally, an oxide layer 44 is disposed over individual floating gates 30, 32, 34, and 36. A plug 46 comprising conductive contact film material is disposed operatively adjacent drain region 42 and serves to electrically connect with such drain region. A barrier layer 48, metal layer 50 and a passivation layer 52 are shown.

The above-described floating gate construction provides an improved floating gate transistor which is less prone to lose its charge due to electron migration from the floating gate through the dielectric layer intermediate the floating gate and the overlying word line. Such

improvements increase the data retention characteristics of the floating gate. The improvements are made possible, in part, through a more uniformly thick bottom oxide layer (oxide layer 20) of the ONO dielectric layer discussed above. Such a uniformly thick layer provides less opportunities for electrons to migrate away from the floating gate.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A method for enhancing data retention of a floating gate transistor comprising:

forming a floating gate over a substrate, the floating gate having an inner first portion and an outer second portion; and

providing conductivity enhancing impurity in the inner first portion to a greater concentration than conductivity enhancing impurity in the outer second portion.

2. The method of claim 1, wherein the forming of the floating gate comprises forming the inner first portion and the outer second portion to comprise polysilicon.

3. The method of claim 1, wherein the floating gate has a thickness, and the forming of the floating gate comprises forming the inner first portion to comprise at least 25 percent of the floating gate thickness.

4. The method of claim 1, wherein the floating gate has a thickness, and the forming of the floating gate comprises forming the inner first portion to comprise between about 25 to 75 percent of the floating gate thickness.

5. The method of claim 1, wherein the providing of conductivity enhancing impurity in the inner first portion comprises doping the inner first portion to a dopant concentration greater than or equal to $1 \times 10^{18} cm^{-3}$.

6. The method of claim 1, wherein the providing of conductivity enhancing impurity in the inner first portion comprises doping the inner first portion to a dopant concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$, with the outer second portion having a dopant concentration of less than $1 \times 10^{18} cm^{-3}$.

7. The method of claim 1, wherein:

the forming of the floating gate comprises forming a first layer of polysilicon over the substrate, the first layer defining the inner first portion, and after the forming of the first layer forming a second layer of polysilicon, the second layer defining the outer second portion.

8. The method of claim 1, wherein:

the forming of the floating gate comprises forming a first layer of polysilicon over the substrate, the first layer defining the inner first portion, and after the forming of the first layer forming a second layer of polysilicon, the second layer defining the outer second portion; and

intermediate the forming of the first and second layers, providing the conductivity enhancing impurity in the inner first portion to a dopant concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

9. A method of forming a floating gate transistor comprising:

forming a first layer of conductively doped semiconductive material over a semiconductive substrate;

forming a second layer of substantially undoped semiconductive material over the first layer;

forming a third layer comprising dielectric material over the second layer;

forming a fourth layer comprising conductive material over the third layer; and

forming a floating gate transistor comprising the first, second, third, and fourth layers.

10. The method of claim 9, wherein the first and second layers comprise a floating gate having a thickness, and the forming of the first and second layers comprise forming the first layer to occupy at least 25 percent of the floating gate thickness.

11. The method of claim 9, wherein the first and second layers comprise a floating gate having a thickness, and the forming of the first and second layers comprise forming the first layer to occupy less than 75 percent of the floating gate thickness.

12. The method of claim 9, wherein the forming of the first layer comprises forming the first layer to have a dopant concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

13. The method of claim 9, wherein the forming of the first layer comprises:

forming a layer of polysilicon over the substrate; and

doping the polysilicon layer with phosphorous dopant material to a concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

14. The method of claim 9, wherein:

the first and second layers comprise a floating gate having a thickness, and the forming of the first and second layers comprise forming the first layer to occupy less than 75 percent of the floating gate thickness; and

the forming of the first layer comprises forming the first layer to have a dopant concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

15. A method of forming a floating gate comprising:

forming a first material over a substrate, the first material having a first average grain size;

forming a second material over the first material, the second material having a second average grain size, the second average grain size being larger than the first average grain size; and

providing the first and second materials into a desired floating gate shape.

16. The method of claim 15, wherein the forming of the first material comprises forming conductively doped polysilicon to have a sheet resistance of between 300 ohm/sq. and 400 ohm/sq..

17. The method of claim 15, wherein:

the forming of the first material comprises forming conductively doped polysilicon to have a sheet resistance of between 300 ohm/sq. and 400 ohm/sq.; and

the forming of the second material comprises forming polysilicon to have a sheet resistance greater than 400 ohm/sq..

18. The method of claim 15, wherein the forming of the first material comprises forming conductively doped polysilicon to have a dopant concentration greater than or equal to about $1 \times 10^{18} cm^{-3}$.

19. The method of claim 15, wherein the forming of the second material comprises forming the second material directly atop the first material.

20. The method of claim 15, wherein the forming of the second material comprises forming the second material directly atop the first material, the first and second materials having a combined thickness of less than or equal to about 1000 Angstroms, the first material having an individual thickness of less than about 75 percent of the combined thickness.

21. A method of forming a floating gate transistor comprising:

forming a floating gate over a substrate, the floating gate comprising a first silicon-containing volume having a first grain boundary area per unit volume, and a second silicon-containing volume over the first silicon-containing volume having a second grain boundary area per unit volume, the second grain boundary area per unit volume being less than the first grain boundary area per unit volume;

forming a dielectric layer over the second silicon-containing volume; and

forming a conductive line over the dielectric layer to provide a floating gate transistor.

22. The method of claim 21, wherein the forming of the dielectric layer comprises forming an oxide layer atop the second silicon-containing volume.

23. The method of claim 21, wherein the forming of the floating gate comprises:

forming a first layer of conductively doped polysilicon over the substrate, the first layer constituting the first silicon-containing volume and having a dopant concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$ and a sheet resistance of between about 300 ohm/sq. and 400 ohm/sq..

24. The method of claim 21, wherein the forming of the floating gate comprises:

forming a first layer of conductively doped polysilicon over the substrate, the first layer constituting the first silicon-containing volume and having a dopant concentration of greater than or equal to about 1 x $10^{18}cm^{-3}$ and a sheet resistance of between about 300 ohm/sq. and 400 ohm/sq.; and

after forming the first layer, forming a second layer of polysilicon over the first layer, the second layer constituting the second silicon-containing volume and having a dopant concentration less than about 1 x $10^{18}cm^{-3}$ and a sheet resistant greater than 400 ohm/sq..

25. A method of forming a floating gate transistor comprising:

forming a first layer of polysilicon over a substrate to a first thickness;

doping the first layer to a degree sufficient to define a sheet resistance of between 300 ohm/sq. and 400 ohm/sq.;

after the doping, forming a second layer of polysilicon over the first layer of polysilicon to a second thickness;

oxidizing the substrate to form a first oxide layer over the second layer of polysilicon;

forming a layer of nitride over the first oxide layer;

oxidizing the substrate to form a second oxide layer over the layer of nitride;

forming a third layer of polysilicon over the second oxide layer; and

etching at least some of the layers to provide a floating gate transistor over the substrate.

26. The method of claim 25, wherein the first and second thicknesses are substantially the same.

27. The method of claim 25, wherein the first and second thicknesses are different.

28. The method of claim 25, wherein the first and second thicknesses comprise an aggregate thickness and the first thickness constitutes less than or equal to about 75 percent of the aggregate thickness.

29. The method of claim 25, wherein the first thickness is less than about 550 Angstroms.

30. The method of claim 25, wherein the first thickness is between 450 Angstroms and 550 Angstroms.

31. The method of claim 25, wherein the forming of the second layer of polysilicon comprises forming the layer to have a sheet resistance which is greater than the sheet resistance of the first layer of polysilicon.

32. A floating gate transistor comprising:

a substrate; and

a floating gate over the substrate having an inner first portion and an outer second portion, the inner first portion being disposed proximate the substrate and the outer second portion being disposed over the inner first portion, the inner first portion containing a concentration of conductivity enhancing impurity which is greater than a concentration of conductivity enhancing impurity contained by the outer second portion;

a dielectric layer disposed over the outer second portion;

a conductive line disposed over the dielectric layer; and

source/drain regions laterally proximate the floating gate.

33. The floating gate transistor of claim 32, wherein the inner first portion contains an impurity concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

34. The floating gate transistor of claim 32, wherein the inner first portion contains an impurity concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$, and the outer second portion contains an impurity concentration of less than $1 \times 10^{18} cm^{-3}$.

35. The floating gate transistor of claim 32, wherein the floating gate has a thickness, and the inner first portion constitutes less than about 75 percent of the floating gate thickness.

36. The floating gate transistor of claim 32, wherein the floating gate has a thickness, and the inner first portion constitutes less than or equal to about 50 percent of the floating gate thickness.

37. A floating gate transistor comprising:

a substrate;

a floating gate over the substrate comprising a first material having a first average grain size and a second material disposed over the first material and having a second average grain size which is larger than the first average grain size;

a dielectric layer disposed over the second material;

a conductive line disposed over the dielectric layer; and

source/drain regions laterally proximate the floating gate.

38. The floating gate transistor of claim 37, wherein the first material has a sheet resistance of less than about 400 ohm/sq..

39. The floating gate transistor of claim 37, wherein the first and second materials define an aggregate thickness and the first material occupies less than 75 percent of the aggregate thickness.

40. The floating gate transistor of claim 37, wherein the first and second material have individual respective thicknesses and the first material thickness is less than the second material thickness.

ABSTRACT OF THE DISCLOSURE

Floating gate transistors and methods of forming the same are described. In one implementation, a floating gate is formed over a substrate. The floating gate has an inner first portion and an outer second portion. Conductivity enhancing impurity is provided in the inner first portion to a greater concentration than conductivity enhancing impurity in the outer second portion. In another implementation, the floating gate is formed from a first layer of conductively doped semiconductive material and a second layer of substantially undoped semiconductive material. In another implementation, the floating gate is formed from a first material having a first average grain size and a second material having a second average grain size which is larger than the first average grain size.

MI22-587

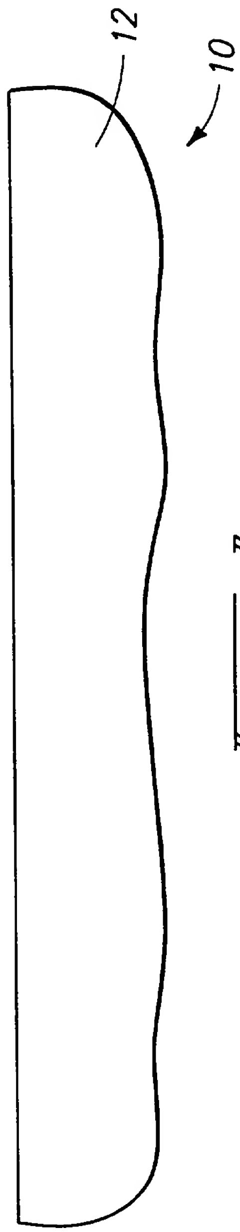

Fig. 1

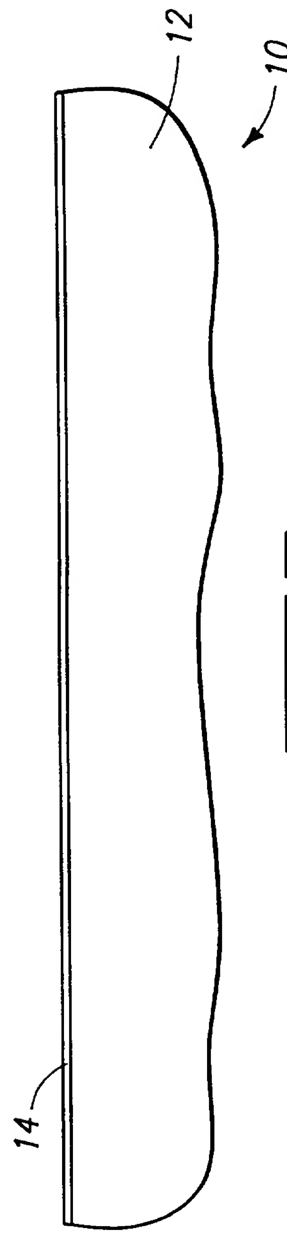

Fig. 2

FIG. 3

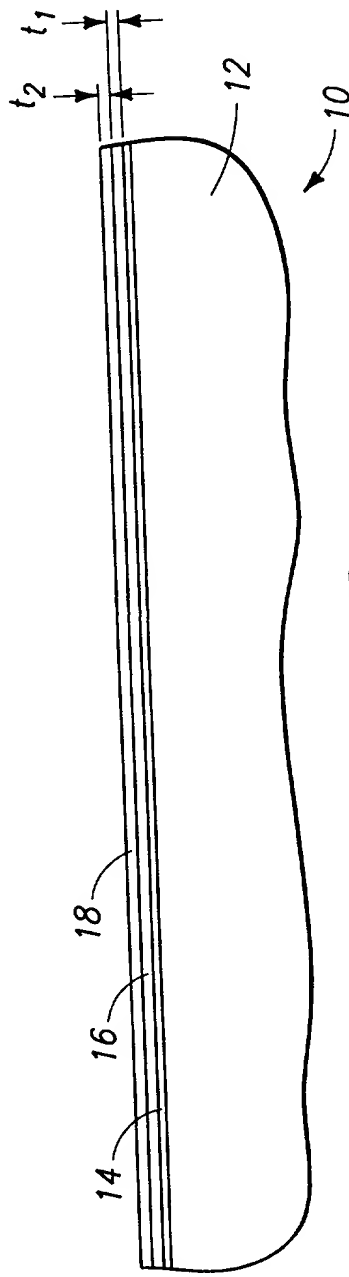

FIG. 4

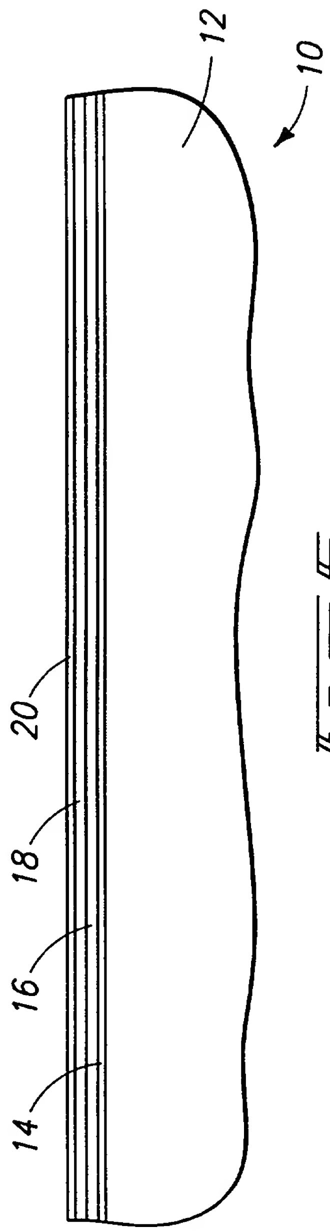

Fig. 5

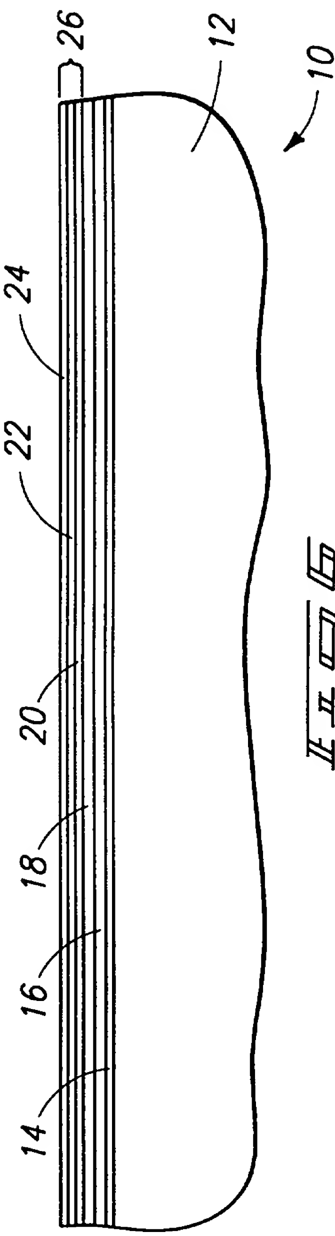

Fig. 6

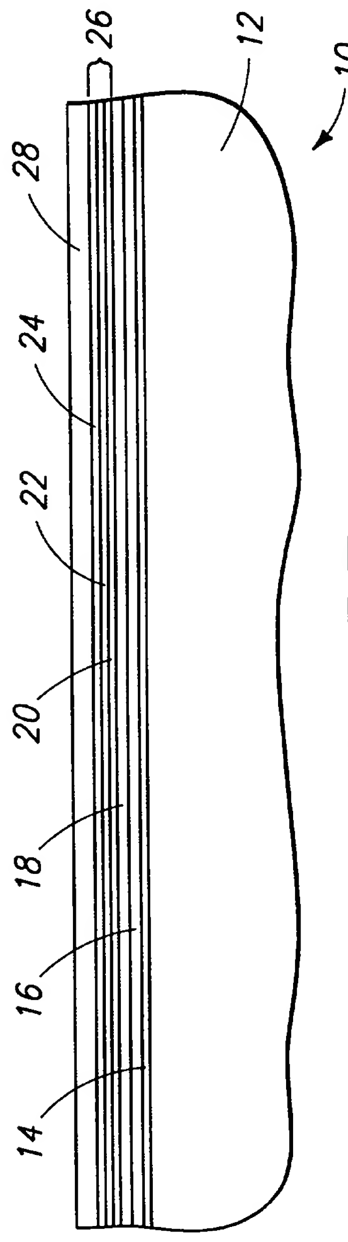
26
12
10
28
24
22
20
18
16
14

FIG. 7

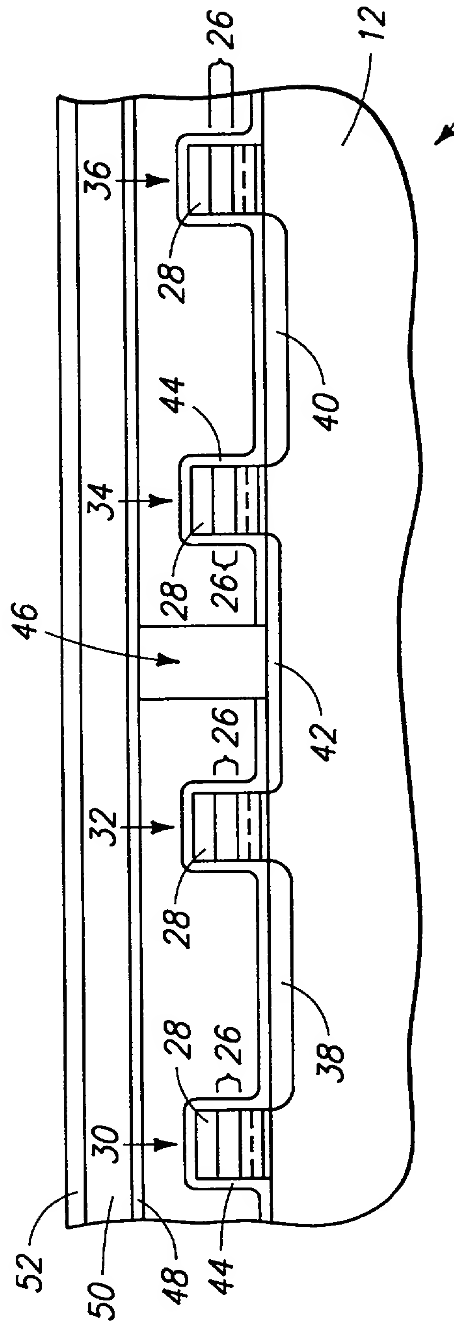
26
12
10
36
28
44
40
34
28
26
46
42
26
32
28
38
28
26
30
52
50
48
44

FIG. 8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor . . . . J. Dennis Keller et al.
Assignee . . . . Micron Technology, Inc.
Attorney's Docket No. MI22-587
Title: Methods of Enhancing Data Retention of a Floating Gate Transistor, Methods of Forming Floating Gate Transistors, and Floating Gate Transistors

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR §3.73(b)

To: Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

MICRON TECHNOLOGY, INC., the Assignee of the entire right, title and interest in the above-identified patent application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of WELLS, ST. JOHN, ROBERTS, GREGORY & MATKIN P.S., listed as follows:

Richard J. St. John	Reg. No. 19,363
David P. Roberts	Reg. No. 23,032
Randy A. Gregory	Reg. No. 30,386
Mark S. Matkin	Reg. No. 32,268
James L. Price	Reg. No. 27,376
Deepak Malhotra	Reg. No. 33,560
Mark W. Hendricksen	Reg. No. 32,356
David G. Latwesen	Reg. No. 38,533
George G. Grigel	Reg. No. 31,166
Keith D. Grzelak	Reg. No. 37,144
John S. Reid	Reg. No. 36,369
Lance R. Sadler	Reg. No. 38,605
James D. Shaurette	Reg. No. 39,833

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia Pappas Dennison (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

EL054830156

The Assignee certifies that the above-identified Assignment has been reviewed and to the best of Assignee's knowledge and belief, title is in the Assignee.

Please direct all correspondence regarding this application to:

Wells, St. John, Roberts, Gregory & Matkin P.S.
Attn: Mark S. Matkin
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3817

Telephone: (509) 624-4276
Facsimile: (509) 838-3424

MICRON TECHNOLOGY, INC.

Dated: 7-13-1998 By: ______

Name: Michael L. Lynch

Title: Chief Patent Counsel

DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Methods of Enhancing Data Retention of a Floating Gate Transistor, Methods of Forming Floating Gate Transistors, and Floating Gate Transistors, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful

EL054830156

false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * *

Full name of inventor: **J. Dennis Keller**

Inventor's Signature: ______________________

Date: 7/1/98

Residence: **Boise, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **1863 S. Londoner Way**
Boise, ID 83706

* * * * * * * * * *

Full name of inventor: **Roger R. Lee**

Inventor's Signature: ______________________

Date: 7-1-98

Residence: **Boise, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **335 ~~Raindrop~~**
~~Boise~~, ID 83706

3936 N. BURNSTEAD
Boise ID 83704